IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

James Chambers

Serial No.:

N/A

Filed:

Herewith

For:

STRUCTURE AND METHOD TO FABRICATE SELF-ALIGNED

TRANSISTORS WITH DUAL WORK FUNCTION METAL GATE

ELECTRODES

Group No.:

N/A

Examiner:

N/A

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

U.S. Patent No.	<u>Inventor</u>	<u>Date</u>
6,534,423 B1	Turner	March 18, 2003
6,397,861 B1	Wing et al.	June 4, 2002
6,383,879 B1	Kizilyalli et al.	May 7, 2002

Foreign Patent No.	Country	<u>Date</u>
GB 2 347 789 A	UK	September 13, 2000

References:

"PURSUING THE PERFECT LOW-K DIELECTRIC"; www.e-insite.net/semiconductor/index.asp?/layout=articlePrint&articleID=CA164243.

B. Maiti and P.J. Tobin; "METAL GATES FOR ADVANCED CMOS TECHNOLOGY"; SPIE Vol. 3881; September 1999; Pgs. 46-57.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 20-0668.

Respectfully submitted,

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Charles W. Gaines

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PTO/SB/08B (08-03) Approved for use through 07/31/2006. OMB 0651-0031

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				Applicati n Number	N/A	
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STA	TEMENT B	BY A	PPLICANT	First Named Inventor James Chambers		
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Sheet	2	of	2	Attorney Docket Number	TI 35714	

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		"PURSUING THE PERFECT LOW-K DIELECTRIC"; www.e-insite.net/semiconductor/index.asp?layout=articlePrint&article ID=CA164243	
		B. Maiti and P.J. Tobin; "METAL GATES FOR ADVANCED CMOS TECHNOLOGY"; SPIE Vol. 3881; September 1999; Pgs. 46-57.	

Examiner	Date	
Signature	Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		First Named Inventor	James Chambers			
		Art Unit	N/A			
		Examiner Name	N/A			
	1		2	Attorney Docket Number	TI 35714	

			U. S. PATENT	T DOCUMENTS	
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ^{2 (f known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,534,423 B1	03 18 2003	Turner	
		^{US-} 6,397,861 B1	06 04 2002	Wing et al.	
		^{US-} 6,383,879 B1	05 07 2002	Kizilyalli et al.	
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		FOREIG	N PATENT DOCU	JMENTS		
Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages	
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)	MM-DD-YYYY		Or Relevant Figures Appear	T ⁶
		GB 2 347 789 A	09/13/2000	NEC Corporation		

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